REMARKS

Reconsideration and allowance of the subject patent application are respectfully requested.

The specification and drawings have been amended, *inter alia*, to correct those informalities noted on page 2 of the office action and to correct other informalities found during preparation of this response. Entry of these amendments is respectfully requested.

Claims 4-12, 16 and 23 were rejected under 35 U.S.C. Section 112, second paragraph, as being indefinite. These claims have been amended to address the various issues identified on pages 2-3 of the office action and withdrawal of this rejection is respectfully requested.

Applicants gratefully acknowledge the indication that claims 14, 15, 21, and 22 contain allowable subject matter. Claims 14 and 21 have been re-written in self-standing independent form and are now believed to be allowable. Claims 15 and 22 depend from claims 14 and 21, respectively, and are also believed to be allowable. The claims have been amended so that claims 2-12 and 16-18 now depend directly or indirectly from claim 14 and so that claim 23 now depends from claim 21. As such these claims are also believed to be allowable.

The above claim amendments do not constitute (and should not be construed to constitute) acquiescence in any outstanding objections or rejections and are done for the purpose of reducing issues in the subject application. Applicants reserve the right to file continuing applications directed to the subject matter of the canceled claims prior to the

termination of proceedings in the subject application or any continuing application based thereon.

New claims 24-39 have been added for the Examiner's consideration. The subject matter of these new claims is fully supported by the original disclosure and no new matter is added. Applicants submit that the subject matter of these new claims is not taught or suggested by the applied art and thus these claims are believed to be allowable.

Applicants submit that the pending claims are allowable and early notice to that effect is respectfully requested.

Respectfully submitted,

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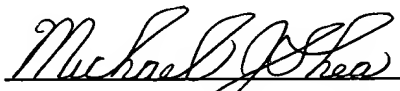
By: 

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Version marked to show changes made

IN THE SPECIFICATION

The paragraph beginning on page 12, line 4 has been amended as follows:

In this example, main processor 110 (e.g., an enhanced IBM Power PC 750) receives inputs from handheld controllers 52 [108] (and/or other input devices) via graphics and audio processor 114. Main processor 110 interactively responds to user inputs, and executes a video game or other program supplied, for example, by external storage media 62 via a mass storage access device 106 such as an optical disk drive. As one example, in the context of video game play, main processor 110 can perform collision detection and animation processing in addition to a variety of interactive and control functions.

The paragraph beginning on page 13, line 6 has been amended as follows:

Graphics and audio processor 114 has the ability to communicate with various additional devices that may be present within system 50. For example, a parallel digital bus 130 may be used to communicate with mass storage access device 106 and/or other components. A serial peripheral bus 132 may communicate with a variety of peripheral or other devices including, for example:

- a programmable read-only memory (PROM) and/or real time clock (RTC) 134,
- a modem 136 or other networking interface (which may in turn connect system 50 to a telecommunications network 138 such as the Internet or other digital network

from/to which program instructions and/or data can be downloaded or uploaded), and

- a flash memory 140.

The paragraph beginning on page 13, line 21 has been amended as follows:

Figure 3 is a block diagram of an example graphics and audio processor 114. Graphics and audio processor 114 in one example may be a single-chip ASIC (application specific integrated circuit). In this example, graphics and audio processor 114 includes:

- a processor interface 150,
- a memory interface/controller 152,
- a 3D graphics processor 154,
- an audio digital signal processor (DSP) 156,
- an audio memory interface 158,
- an audio interface and mixer 1300 [160],
- a peripheral controller 162, and
- a display controller 164.

The paragraph beginning on page 14, line 8 has been amended as follows:

3D graphics processor 154 performs graphics processing tasks. Audio digital signal processor 156 performs audio processing tasks. Display controller 164 accesses image information from main memory 112 and provides it to video encoder 120 for display on display device 56. Audio interface and mixer 1300 [160] interfaces with audio

code 122, and can also mix audio from different sources (e.g., streaming audio from mass access storage device 106, the output of audio DSP 156, and external audio input received via audio codec 122). Processor interface 150 provides a data and control interface between main processor 110 and graphics and audio processor 114.

The paragraph beginning on page 17, line 20 has been amended as follows:

Texture unit 500 outputs filtered texture values to the texture environment unit 600 for texture environment processing (600a). Texture environment unit 600 blends polygon and texture color/alpha/depth, and can also perform texture fog processing (600b) to achieve inverse range based fog effects. Texture environment unit 600 can provide multiple stages to perform a variety of other interesting environment-related functions based for example on color/alpha modulation, embossing, detail texturing, texture swapping, clamping, and depth blending.[.]

The paragraph beginning on page 18, line 3 has been amended as follows:

Pixel engine 700 performs depth (z) compare (700a) and pixel blending (700b). In this example, pixel engine 700 stores data into an embedded (on-chip) frame buffer memory 702. Graphics pipeline 180 may include one or more embedded DRAM memories 702 to store frame buffer and/or texture information locally. Z compares 700a' can also be performed at an earlier stage in the graphics pipeline 180 depending on the rendering mode currently in effect (e.g., z compares can be performed earlier if alpha blending is not required). The pixel engine 700 includes a copy operation 700c that periodically writes on-chip frame buffer 702 to <u>memory portion 113 of</u> main memory 112

for access by display/video interface unit 164. This copy operation 700c can also be used to copy embedded frame buffer 702 contents to textures in the main memory 112 for dynamic texture synthesis effects. Anti-aliasing and other filtering can be performed during the copy-out operation. The frame buffer output of graphics pipeline 180 (which is ultimately stored in main memory 112) is read each frame by display/video interface unit 164. Display controller/video interface 164 provides digital RGB pixel values for display on display 56.

The text beginning on page 18, line 19 and continuing to page 19, line 4 has been amended as follows:

Example Input/Output Subsystem [Peripheral Controller]

Figure 6 shows an example input/output subsystem [peripheral controller 162]. In this example, the input/output subsystem [peripheral controller 162] includes a serial interface 1000, an external interface 1100, a disk interface 1200 and an audio interface 1300. Serial interface 1000 is used to communicate with controllers 52 or other devices that can be coupled to one of four serial ports of system 50. External interface 1100 is used to communicate with a variety of devices such as PROM RTC 134, modem 136, flash memory 140, memory card 144, etc. via various buses 132, 142. Disk interface 1200 is used to communicate with mass storage access device 106 via a parallel bus 130. Audio interface 1300 is used to stream the audio output data from an audio buffer in main memory 112 to audio codec 122.

The paragraph beginning on page 19, line 5 has been amended as follows:

In the example embodiment, the external interface 1100 and disk interface 1200 have direct access to memory controller 152 via a bus 900. Details of the operation of memory controller 152 may be found in provisional Application No. 60/226,894, filed August 23, 2000 and its corresponding utility Application No. 09/726,220, filed November 28, 2000 [_____, filed _____ (atty. dkt. no. 723-974)], both entitled "Graphics Processing System with Enhanced Memory Controller" and provisional Application No. 60/226,886, filed August 23, 2000 and its corresponding utility Application No. 09/722,665, filed November 28, 2000 [_____, filed _____ (atty. dkt. no. 723-970)], both entitled "Method and Apparatus for Accessing Shared Resources." The contents of each of these applications are incorporated herein by reference. In addition, each one of interfaces 1000, 1100, 1200 and 1300 as well as audio digital signal processor 156 share a common bus 902 used to communicate between these components and a bus interface 904. The bus interface 904, in turn, can be used to arbitrate access to graphics unit 180. In the example embodiment, there is also a connection 906 between DSP 156 and audio interface 1300.

The paragraph beginning on page 35, line 25 has been amended as follows:

Figure 10 shows details of one of controllers 52. Controller 52 is connected to serial interface 1000 via a cable (not shown) about 2 meters in length in the example system. In other implementations, the communication between the controllers and the console may be over a wireless communication path such as infrared or radio frequency. Controller 52 contains an interface circuit 1504 arranged between the controller

components and serial interface 1000. A button data input circuit 1502 accepts inputs from buttons disposed on an external surface of controller 52. "Buttons" as used herein refers to any device that is manipulable by a user to cause a game or other application to start, characters to move, etc. and includes, for example, buttons, switches, joysticks, and the like. The length of the controller button and status data that is provided to serial interface 1000 is 64 bits. Vibration circuit 1506 is responsive to signals from main unit 54 via serial interface 1000 for selectively vibrating the housing of controller 52 to provide sensations to the a game player. Controller 52 also includes a 64 kbit EEPROM 1510 with a unique identifier number that is usable, for example, to store game back-up data, high game scores, etc. Controller 52 also includes a motor control system 1508 [1506] for controlling an external motor and two output ports (not shown) connectable to external components such as a motor.

IN THE CLAIMS

Claims 2-4, 6, 7, 14, 16-18, 21 and 23 have been amended as follows:

2. (Amended) The video game system according to claim 14 [1], wherein the interface is programmable to poll the controllers a predetermined number of times between each vertical blanking interval.

3. (Amended) The video game system according to claim 14 [1], wherein the interface is programmable to poll the controllers based on a number of video lines.

4. (Amended) The video game system according to claim 14 [1], wherein the interface polls a [the] status of the controllers.

6. (Amended) The video game system according to claim 5 [4], wherein the player inputs comprise button presses.

7. (Amended) The video game system according to claim 5 [4], wherein the player inputs comprise positions of a user manipulable joystick.

14. (Amended) A [The] video game system [according to claim 13], [the interface further] comprising:

a game program executing system executing a game program;

one or more controllers supplying user inputs to the game program executing system;

an interface between the controllers and the game program executing system, the interface system being programmable to periodically poll the controllers without involvement of the game program executing system, wherein the interface comprises:

a double buffer for storing data transferred between the game program executing system and the controllers; and

a communication RAM for storing data transferred between the game program executing system and the controllers [controller].

16. (Amended) The video game system according to claim 14 [1], the interface further comprising:

a modem [for pulse width modulating/demodulating data transferred between the game program executing system and the controller].

17. (Amended) The video game system according to claim 14 [1], the controller including a vibration circuit for vibrating a housing of the controller.

18. (Amended) The video game system according to claim 14 [1], the controller including a read/write memory.

21. (Amended) A [The] video game system [according to claim 20], [the interface further] comprising:

a game program executing system executing a game program;

a controller supplying user inputs to the game program executing system; and

an interface interfacing between the game program executing system and the controller, the interface including communication circuitry operable in a first mode in which data of a fixed size is communicated between the game program executing system and the controller and in a second mode in which data of variable size is communicated between the game program executing system and the controller, wherein the interface further comprises:

a communication memory for storing the variable size data; and

a double buffer for storing the fixed size data.

23. (Amended) The video game system according to claim 21 [19], the interface further comprising:

a modem [for pulse width modulating/demodulating data transferred between the game program executing system and the controller].